ELE660 – RF Power Amplifiers for Wireless and Satellite Communications

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Department of Electrical Engineering

College of Engineering

Project I

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Introduction

Project is aimed to design a class AB amplifier using GAN technology of transistor CGH40010F. It is intended to operate at a frequency of 2.1 GHz, and a bias condition of conduction angle of 270 degrees. There were five main objectives for the project. First, DC biasing study in which ideal bias point to be chosen. Second, DC feed design that needed to figure out the DC feed and DC block for the circuit. Third, conducting a stability simulation for the intended frequency in which S-parameters sweep was used to get a value for a series resistor at the transistor gate to ensure the stability of transistor. Fourth, Load Pull technique was done using existing ADS design guide to get the output and input reflection coefficients that will be used to design a matching network for the Power Amplifier design. Finally, one tone and two-tone analysis to be conducted to study the performance on the overall design and to compare it to the datasheet provided.

Ideal DC simulation

The first step in the design is to find an ideal bias point such that the transistor is biased as a class AB amplifier operating with a conduction angle of 270 degrees. A conduction angle of 270 degrees translates to the amplifier conducting for ¾ of the period at the frequency of operations. For the design, the center frequency was specified as 2.1 GHz which translates to 476.19ps. Hence, it is expected that the drain current waveform will be clipped to zero for ¼ of the full period which is approximately 120ps. Hence, the correct bias point needs to be picked to achieve this desired performance. After revising the datasheet, VDS was fixed at 28V and VGS was varied to achieve the bias point. A quick sweep of VGS with a constant VDS produces Figure 1 which is the drain current vs VGS. The drain current saturates at around 1.431A which approximately matches the maximum drain current of 1.5A as specified by the datasheet. To bias the transistor to work as a class AB amplifier with a 270

degrees conduction angle, the quiescent drain current point will be chosen such that drain current will be forced to zero for 90 degrees.

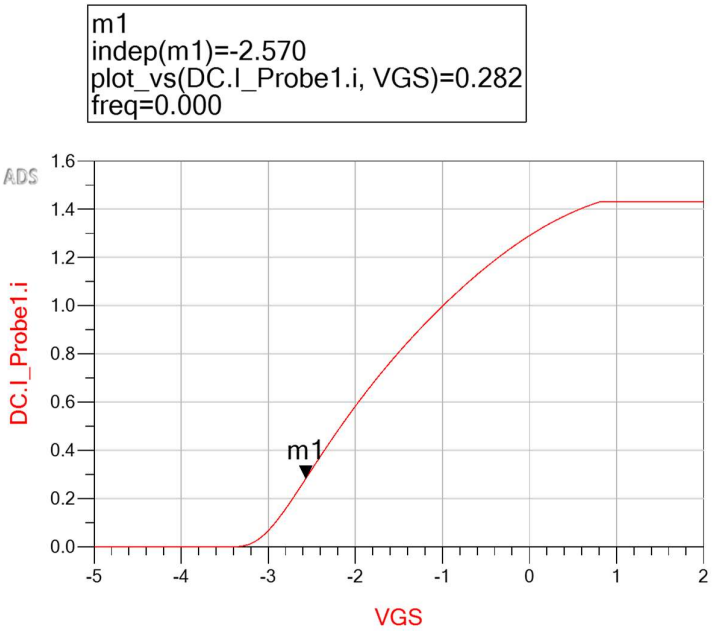


Figure 1. drain current vs VGS.

After sweeping VGS with a constant VDS=28V, the best VGS was found as -2.57V as it resulted in the transistor's drain current clipping for a period of around 120ps, as seen in figure 4, when a 23.5dBm signal at 2.1 GHz is applied using the schematic shown in figure 3.

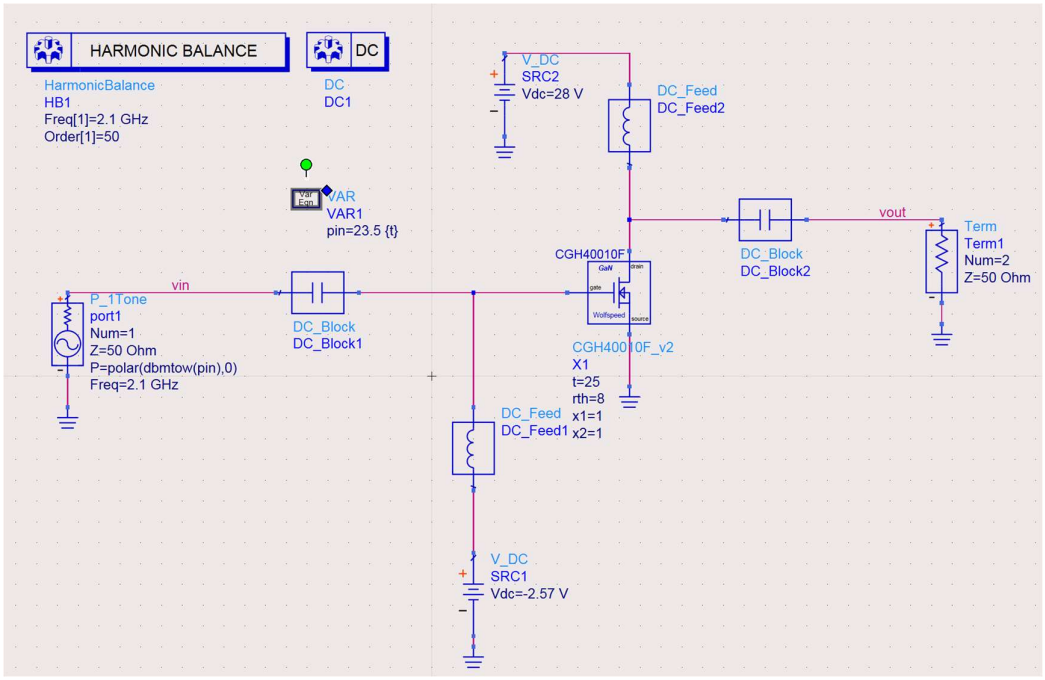


Figure 3. Ideal DC simulation schematic.

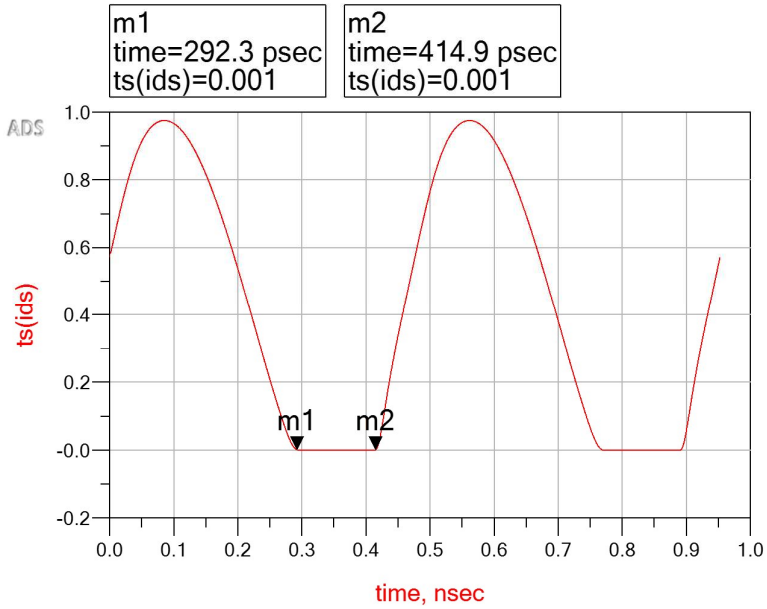


Figure 4. drain current vs time plot with VGS=-2.57.

DC Feed Design

The first simulation was done using ideal DC feeds and DC blocks; however, the actual design requires building a somewhat realistic simulation that utilizes capacitors and transmission lines. The DC block is essentially a short circuit for high frequencies and an infinite impedance for DC. This is done by choosing the highest available capacitance value which is 10000pF such that the impedance at 2.1GHz is 0.00758 ohms. The DC feed on the other hand requires a short circuit that is transformed into an open circuit using a λ/4 transmission line transformer. This is achieved by using the same 10000pF capacitor and tuning a transmission line such that the combination appears as an open circuit as seen in figure 6.

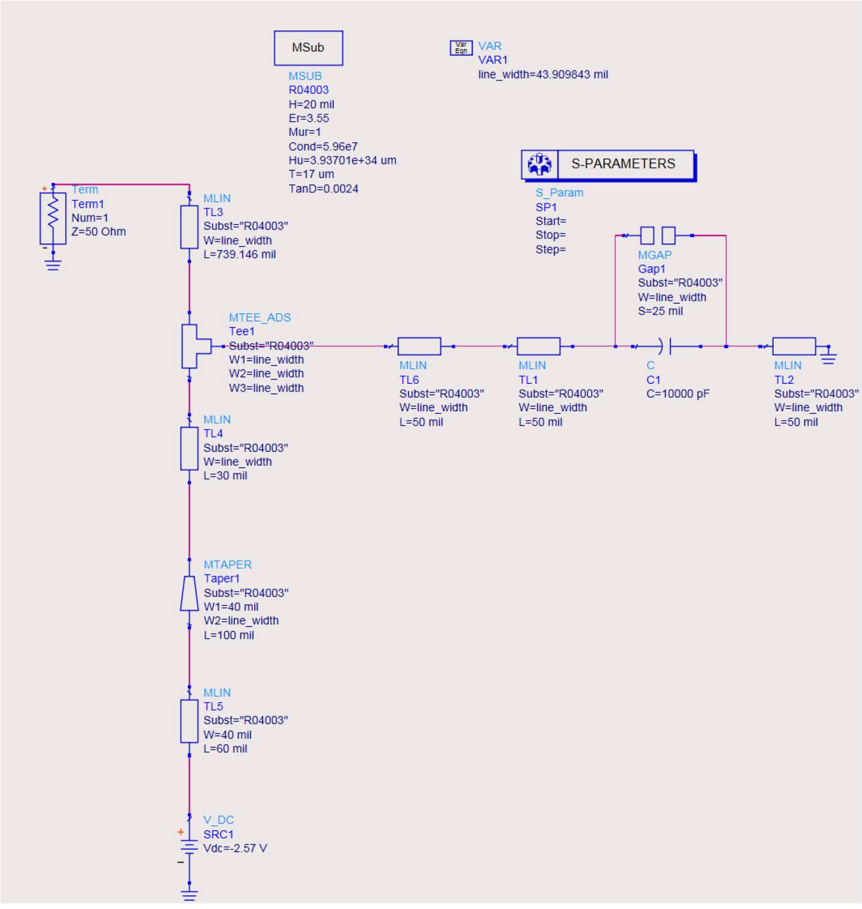


Figure 5. DC Feed network.

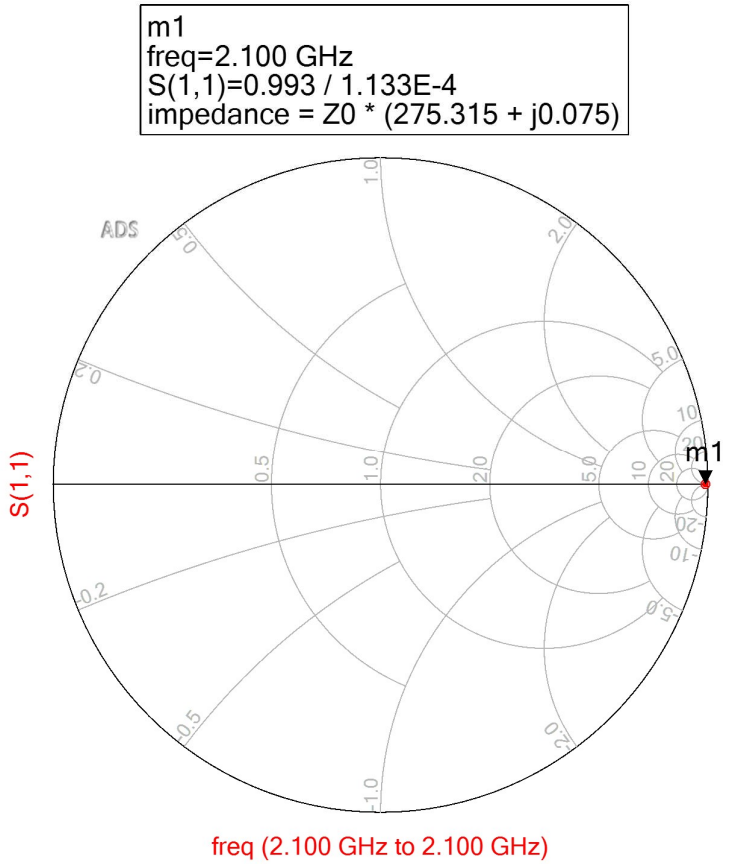


Figure 6. DC Feed network reflection coefficient at 2.1 GHz.

Real DC simulations

The ideal Dc Feed and DC block were replaced in the initial schematic with the designed feed network and dc block. In addition, the effect of the soldering pads of the transistor was simulated by adding transmission lines to mimic the soldering pads of the transistor's gate and drain pins. Figure 7 shows the ADS schematic and figure 8 indicates that the addition of the non-ideal elements corrupts the waveform compared to the ideal simulation, but the dc bias requires no change to maintain a conduction angle of 270 degrees.

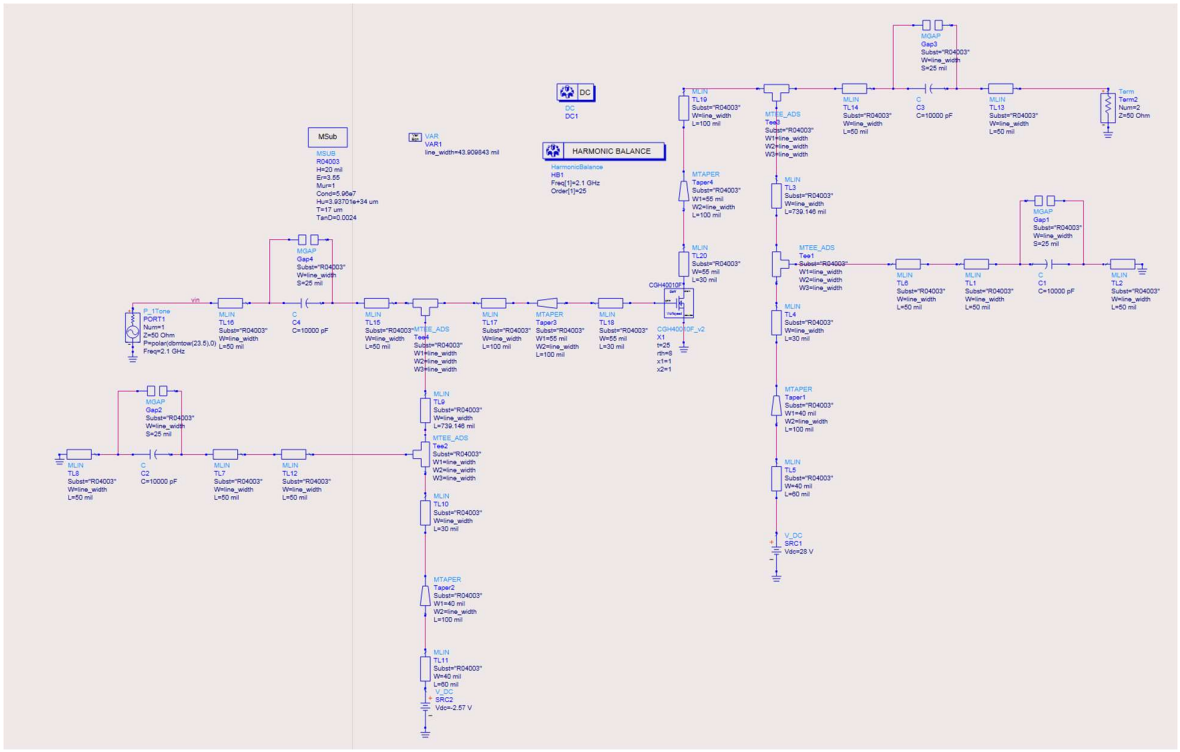


Figure 7. Full DC biasing schematic

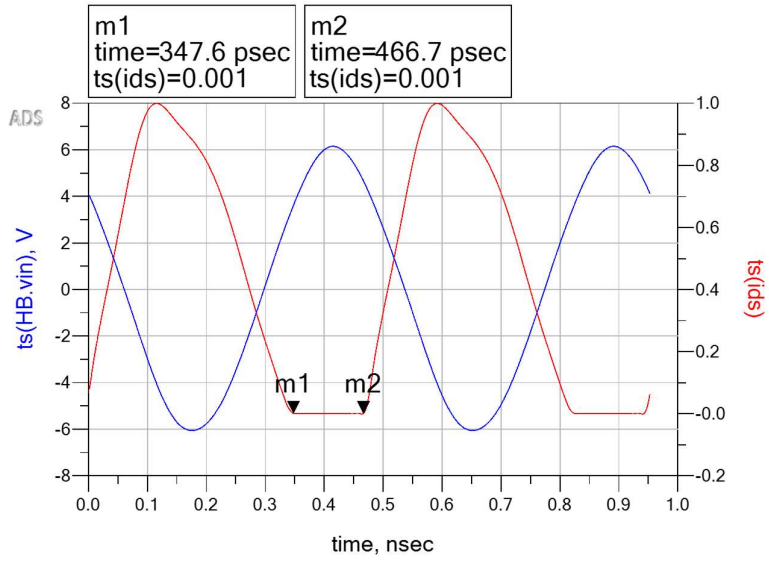


Figure 8. non-ideal DC simulations drain current waveform.

Stability Analysis

For the amplifier to be stable for 10% of its operating frequency, an S parameters sweep was performed with the addition of a series resistor in the gate side of the transistor. The resistor value was tuned such that the transistor is stable throughout the desired frequency range from 1.995 GHz to 2.205 GHz. Figure 10 shows the input and output stability circles plotted on one smith chart. The resistor value was set to 2.44 ohms to achieve stability.

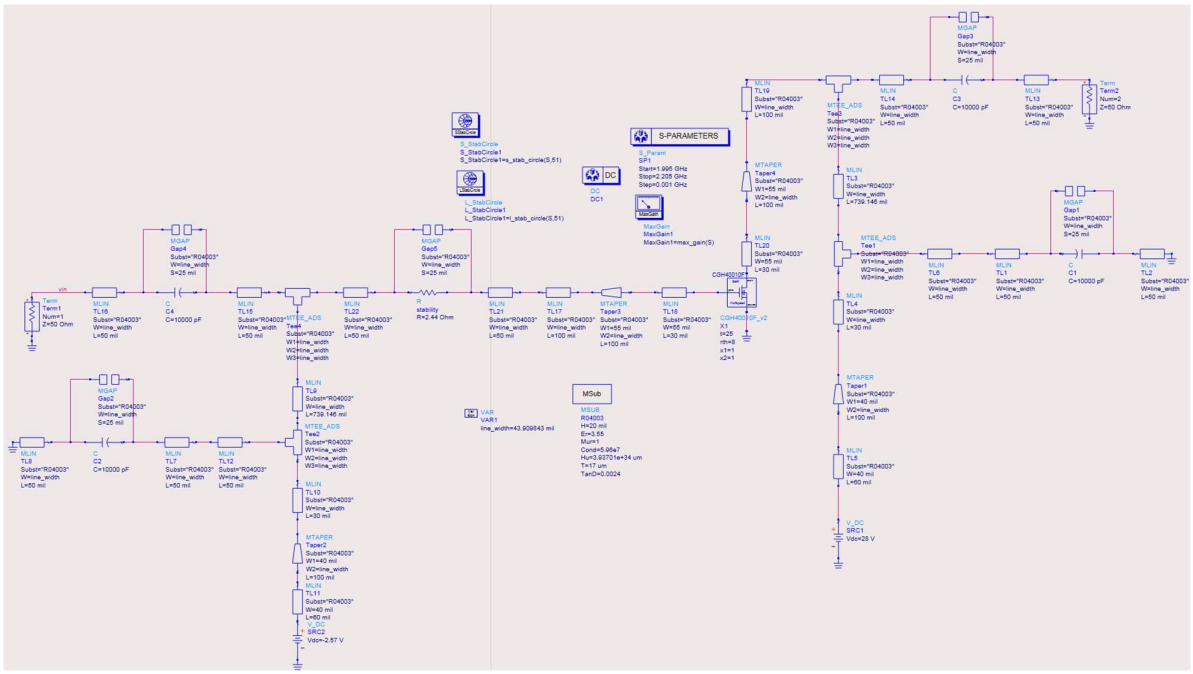


Figure 9. stabilized amplifier plot.

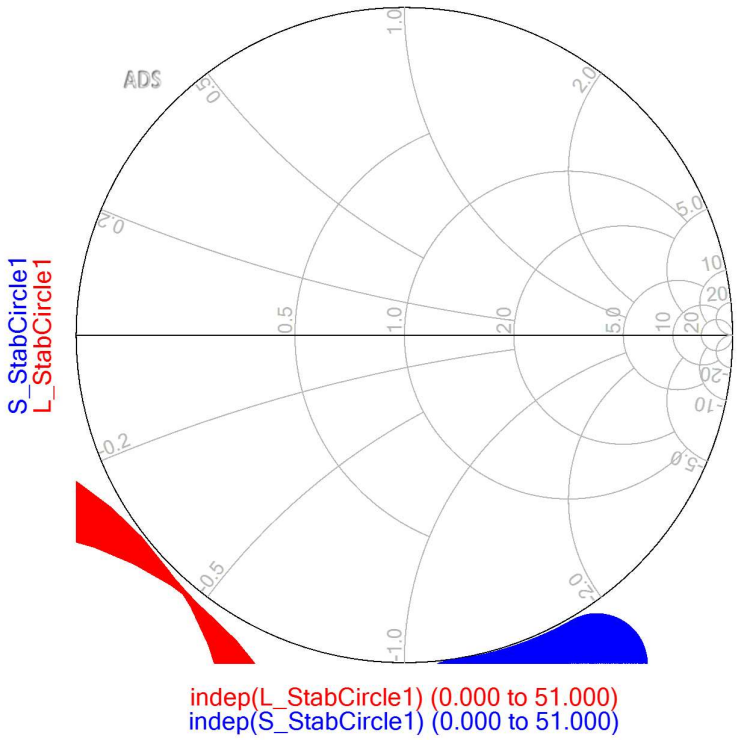


Figure 10. source and load stability circles.

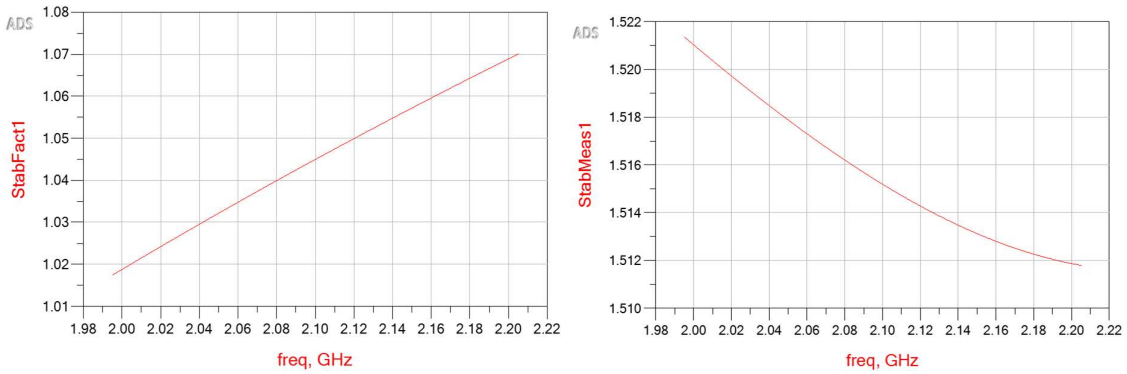


Figure 11. stability measure and stability factor.

Load Pull Results

For the load pull simulations, the load impedance of the stabilize transistor was swept using one of the built in ADS design guides. The design requirements state that the amplifier is to have maximum power output which corresponds to designing the power amplifier such that it can reach its saturation power. According to the datasheet, the saturation power of the amplifier is 13W at 2.1GHz. Hence, the load pull simulation was to be tuned such that the maximum output power of the amplifier is around 13W. Figure 13 shows the results of the load pull simulation. For a maximum power of 41.189dBm, the optimum load reflection coefficient was calculated as 0.465 <-119.668. the input impedance of the device at this operating condition is 7.596+ j65.53. This was achieved when the amplifier was fed with a 29.55 dBm input signal. Hence a source impedance matching network with the complex conjugate of the input impedance is to be built and an output impedance matching network that results in the maximum power output as specified is to be built.

It was noticed that the device model used in ADS saturates at 42.77 dBm with a single tone which is around 19W. Thus, this value was ignored as the transistor is specified to saturate at 13W.

It was noted that the values calculated by ADS in the Load pull schematic assume that there is no input impedance matching network. Thus, the small signal gain was found as 13.7dB which is much lower than the maximum gain of the amplifier that is around 20 dB. Thus, the load pull analysis results are just used as a reference to design the input and output impedance matching networks for maximum output power, and it is expected that the small signal gain and the maximum input power will change.

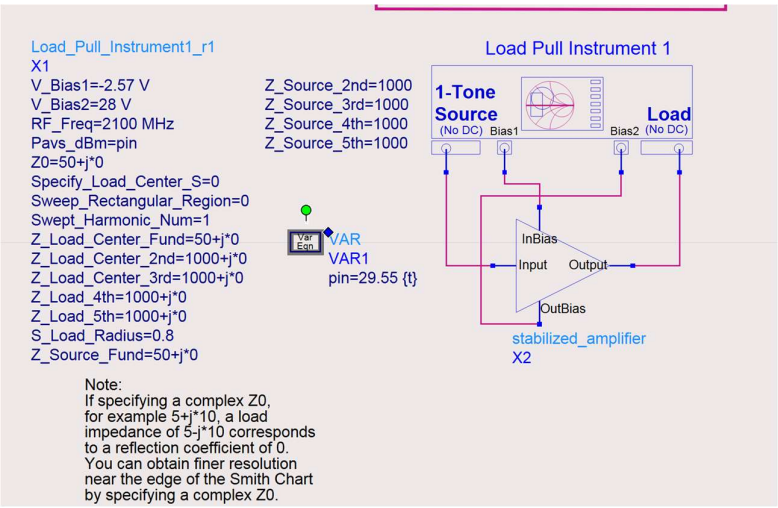


Figure 12. load pull simulation schematic.

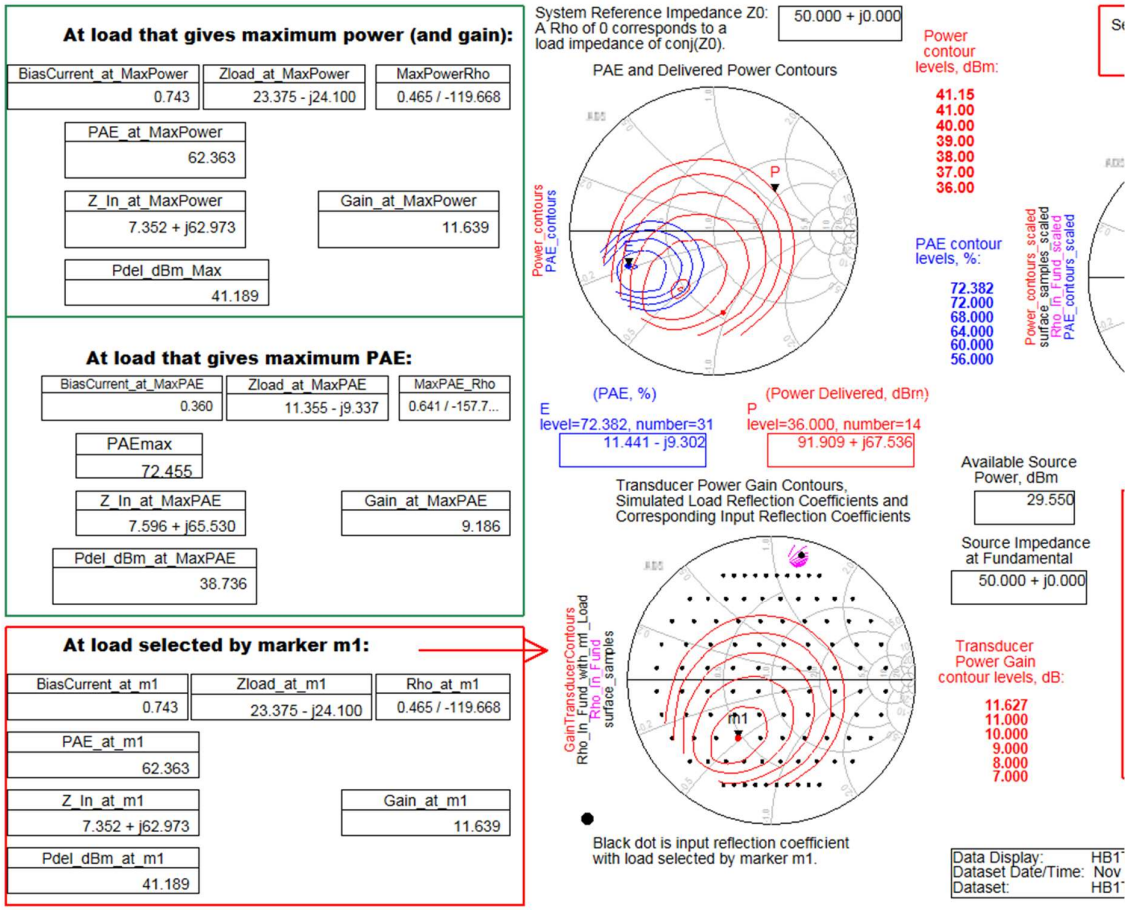


Figure 13. Load Pull analysis results without input impedance matching network.

Output Impedance Matching Network

The output impedance matching network was built using a stub transmission line to almost meet the desired 0.465 <-119.668 load reflection coefficient.

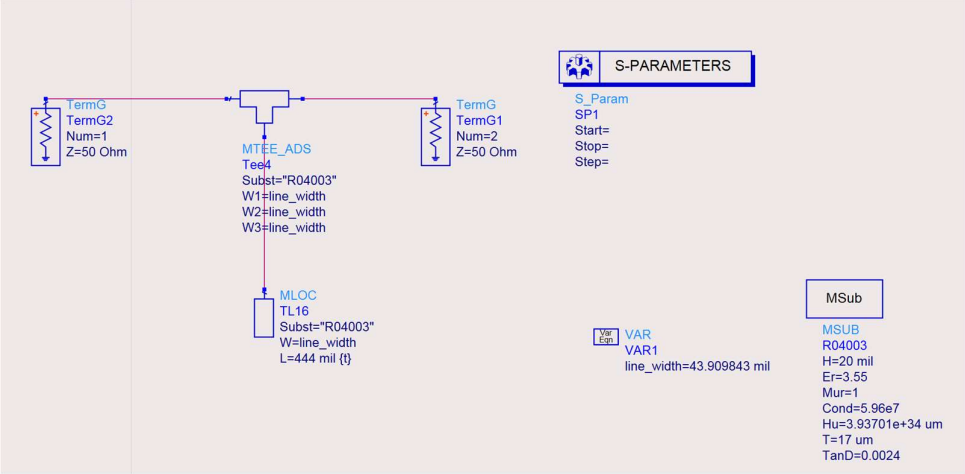


Figure 14. output impedance matching network

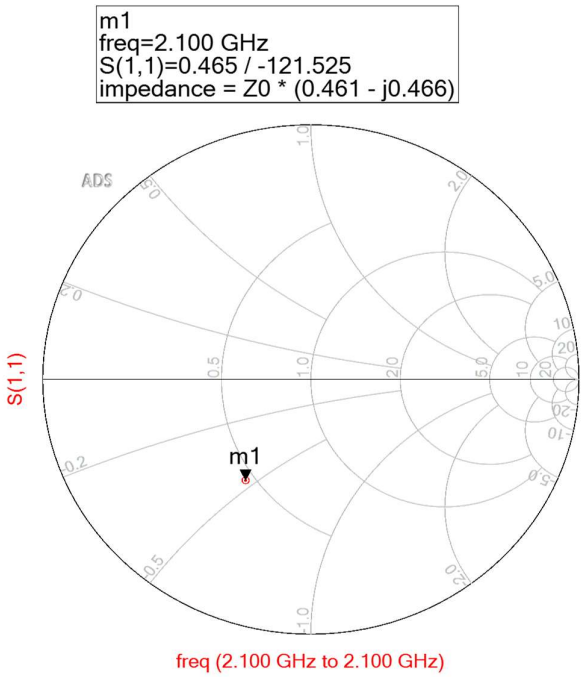


Figure 15. S11 of the output impedance matching network

Input Impedance Matching Network

The input impedance matching network was designed to show the amplifier a normalized input impedance=0.147- j1.259.

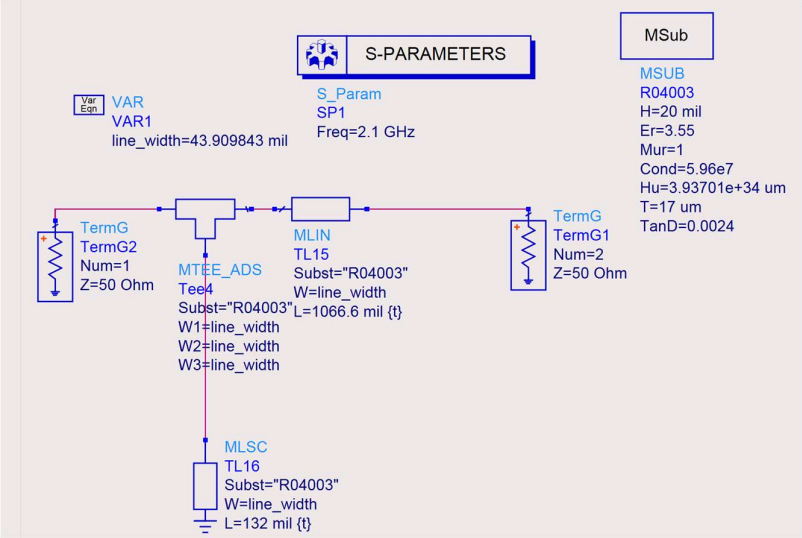


Figure 16. input impedance matching network.

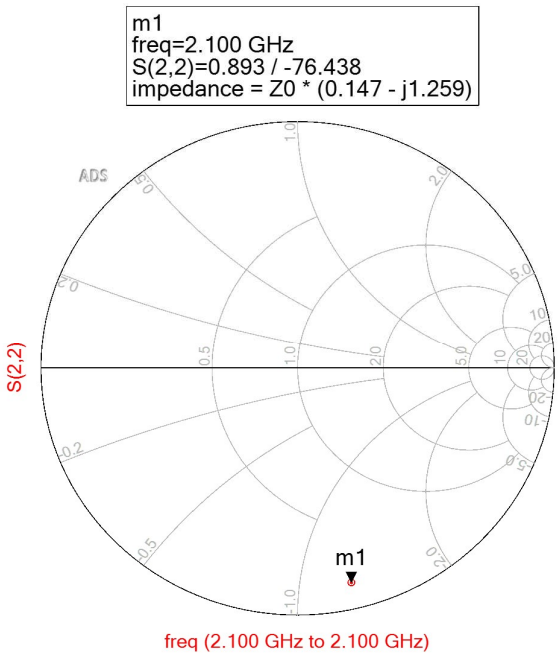


Figure 17. input impedance matching network reflection coefficient.

One-Tone simulations

A 1-tone simulation was performed with the full amplifier including the impedance matching networks. It can be noted that the amplifier appears to saturate at 42.5 dBm, however the datasheet's specified 41.13 dBm will be used for analysis. The amplifier saturates at an input power of 23.35 dBm according to the 1-Tone simulation. This corresponds to a gain compression of around 1.81 dB. The amplifier has a small signal gain of around 19.5 dB.

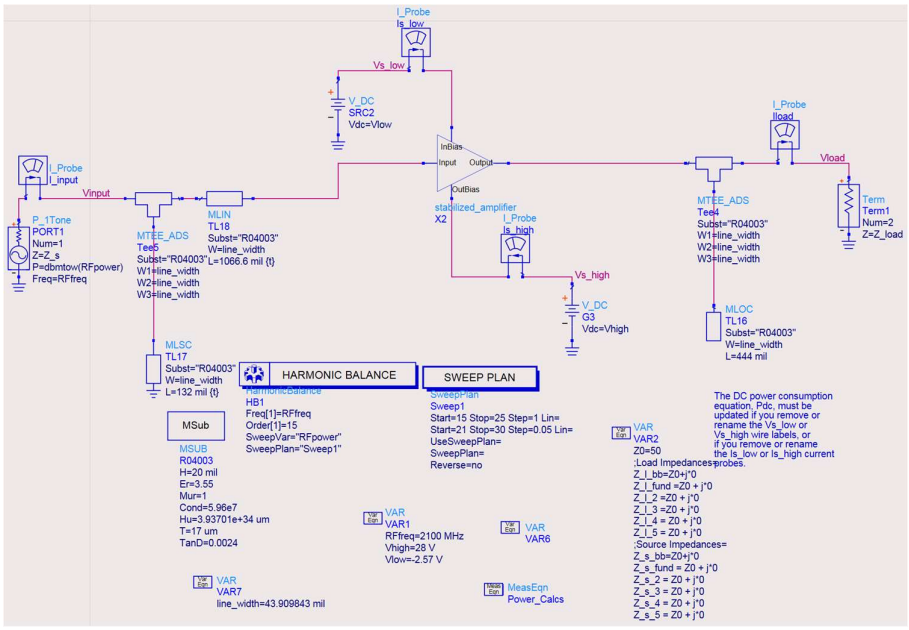


Figure 18. one tone simulations settings.

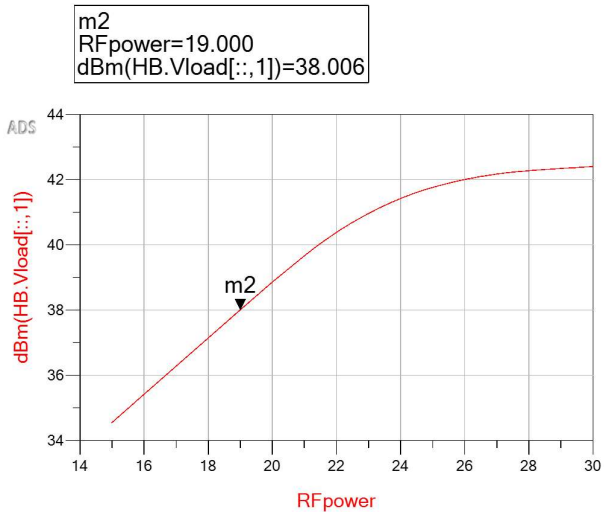


Figure 19. output power vs input power.

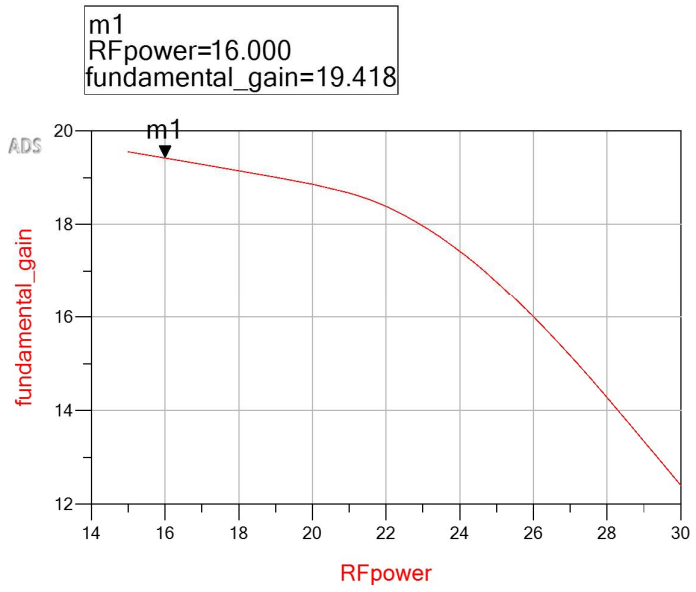


Figure 20. AM-AM plot.

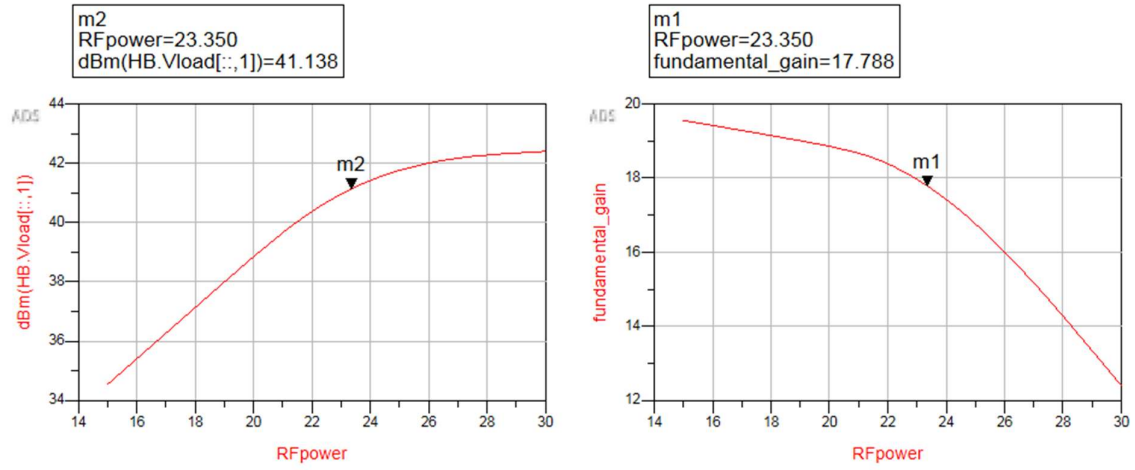


Figure 21. Psat gain and corresponding input power.

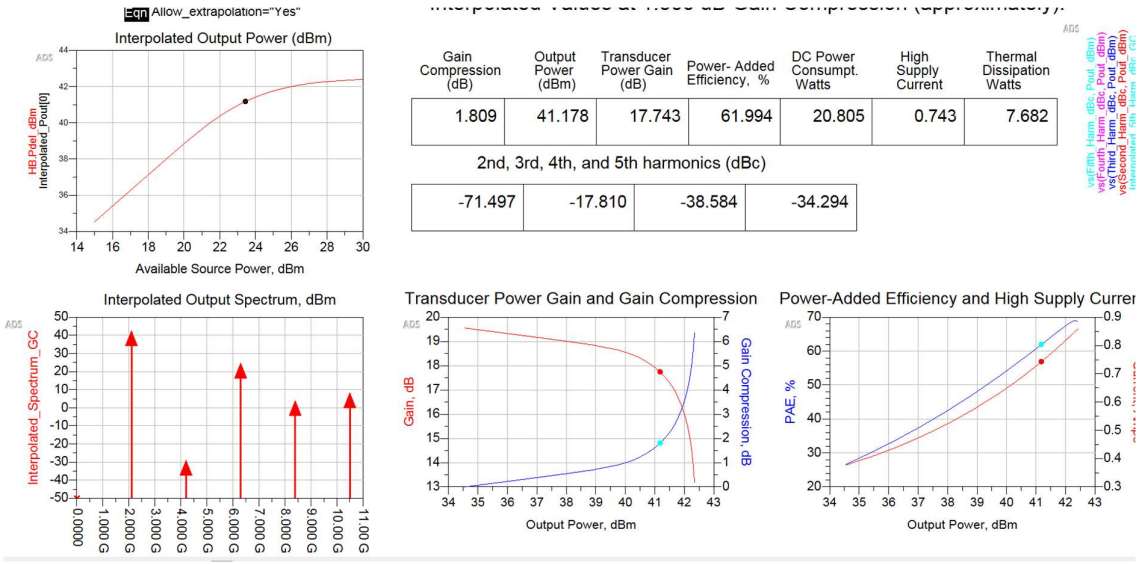


Figure 22. gain compression at saturation.

Two Tones simulation

The results of the two-tone simulation are comparable to the one tone simulation in terms of small signal gain as the small signal gain was found as 19.8dB. The amplifier saturates at a total input power or around 28.6 dBm which is higher than that of the one tone simulation. This was because the gain compression at the saturation power is around 7.307 dB to result in a small signal gain of 12.528 dB. The amplifier has a power added efficiency of 58.66% at this operating output power which is only 3% less than the efficiency projected by the load pull analysis. Further, the two-tone test results indicate that the power amplifier saturates at around 41.3 dBm which matches the datasheet specified saturation power. In addition, the values of CIMD3(12.125 dBc) and CIMD5(19.2 dBc) further indicate that the amplifier is saturating due to the high non-linearities. Hence, the two-tone signal produced a more realistic simulation about the amplifier operation, and it also provided a way of quantifying the effect of the non-linearity at higher output powers through the intermodulation.

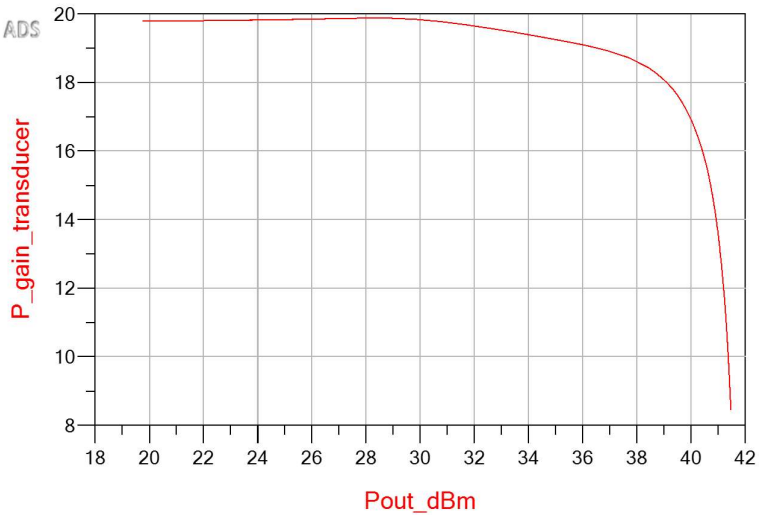


Figure 23. transducer gain vs output power.

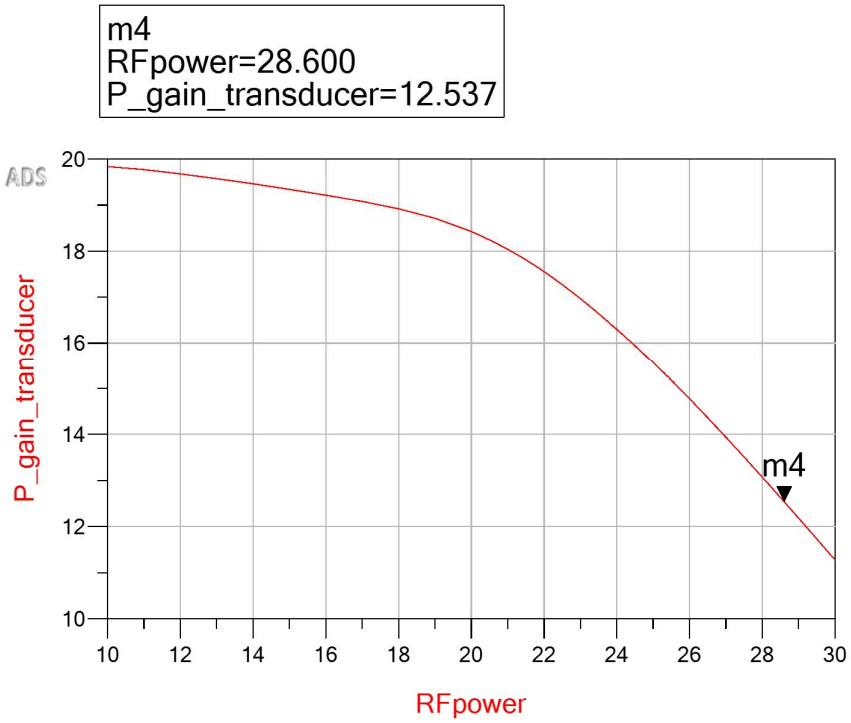


Figure 24. 2 Tone AM-AM plot.

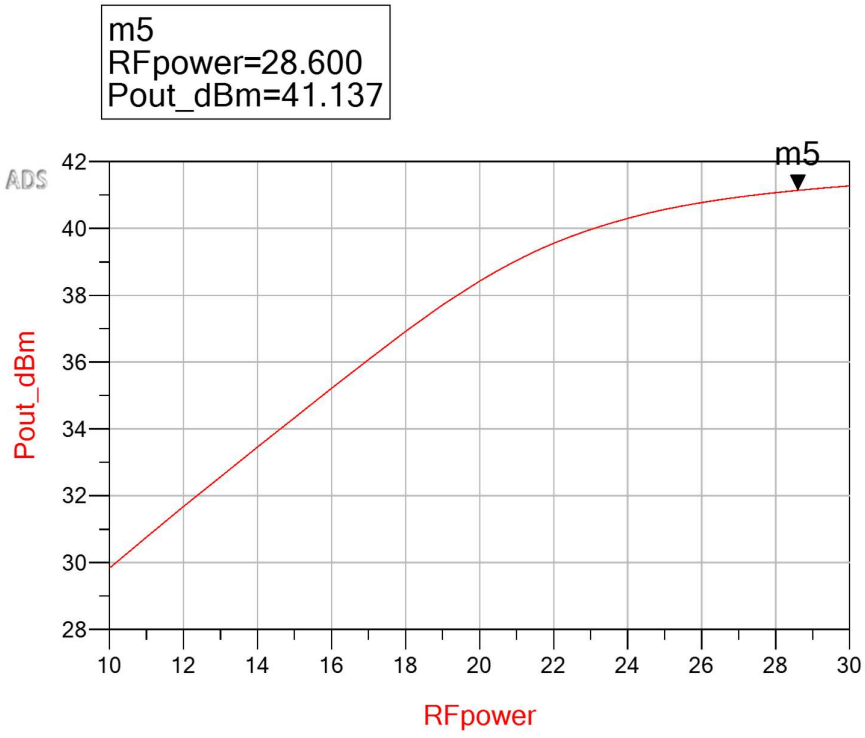


Figure 25. 2 tone total fundamental pout vs pin plot.

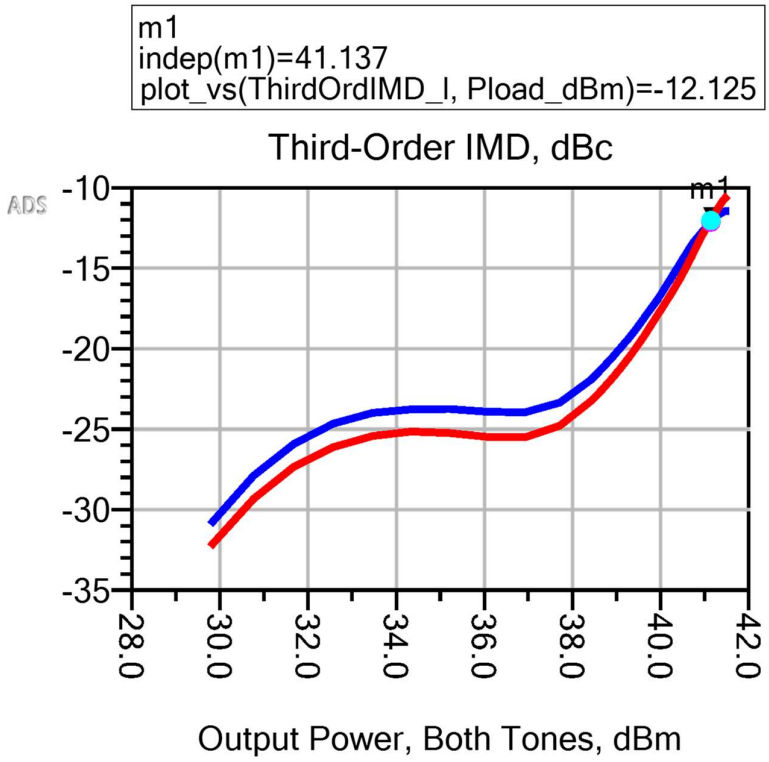


Figure 26. CIMD3 vs output power.

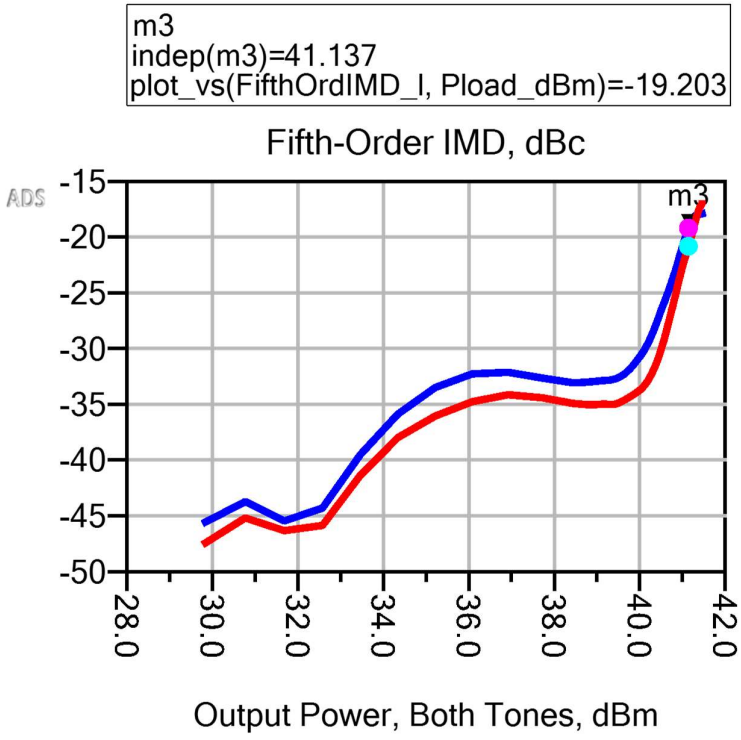
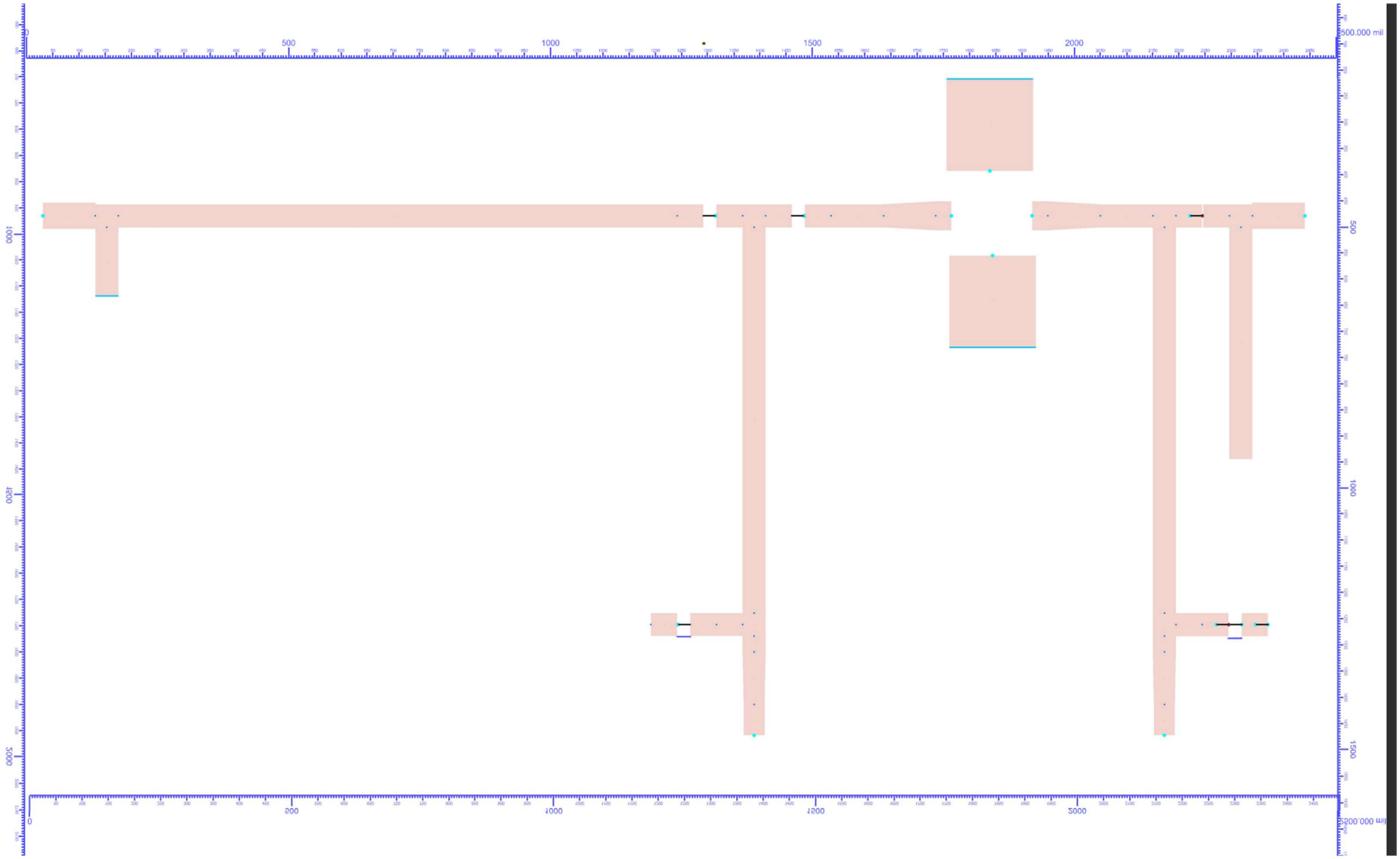


Figure 27. CIMD5 vs output power.

Layout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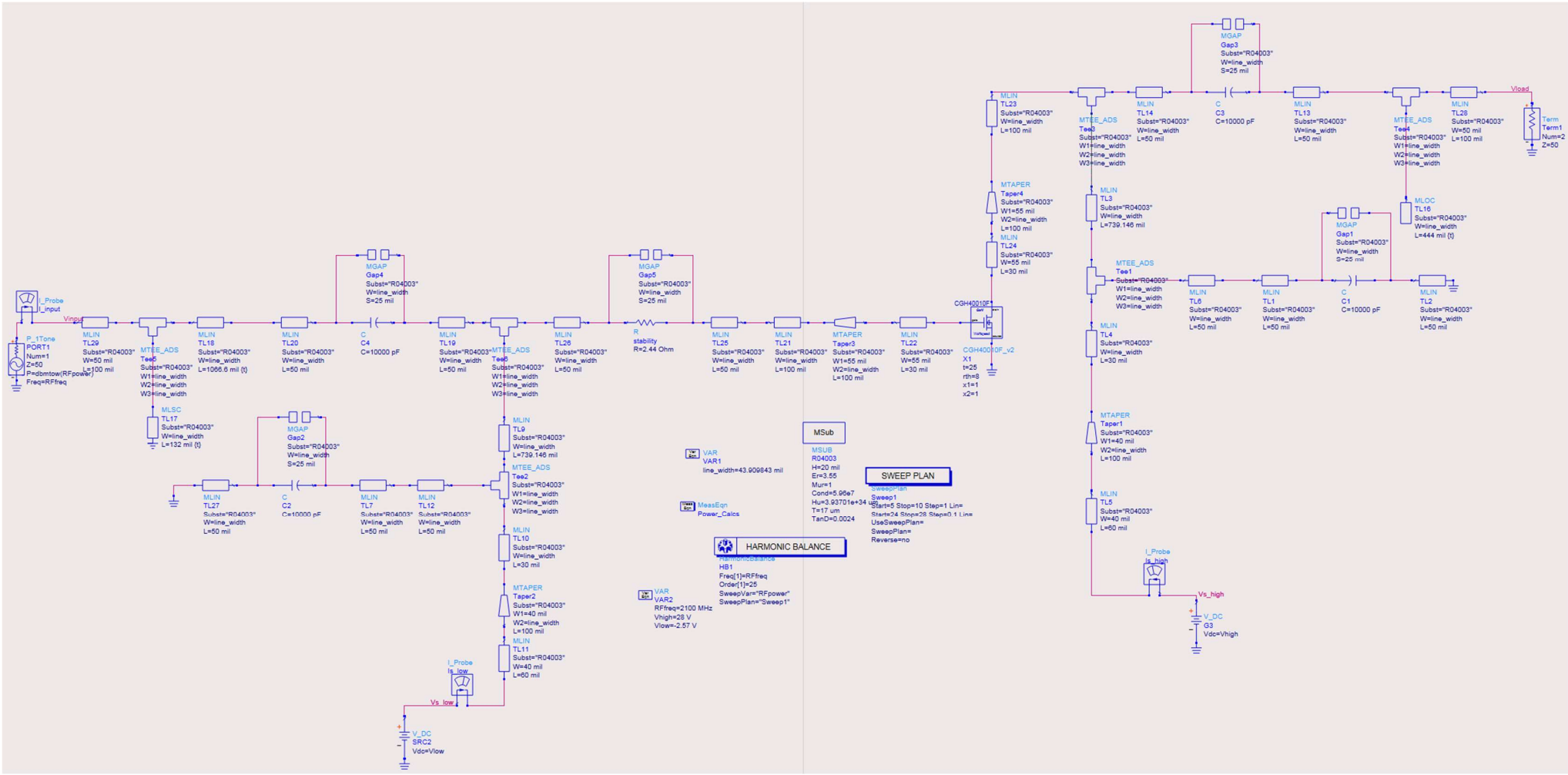
Full schematic



Conclusion

To conclude, the report shows the steps taken to achieve the objectives of the project and to study the amplifier design performance. Stability analysis ensured operating over range of 1.995 GHz to 2.205 GHz frequencies. The project showed the use of ADS existing design guides that helped in performing a load pull simulation. Furthermore, implementing matching network and tones simulation to ensure and study the stability of Power Amplifier design were conducted and analyzed. In addition to the project objectives, the amplifier design included a circuit layout.

Final Data sheet

VGS=-2.57V VDS=28V ID=0.282mA

Unconditional stability range: 1.995 GHz to 2.205 GHz

Small signal gain at 2.1 GHz= 19.8 dB

Saturation power=13 W

Compression at saturation power=7.3 dB

PAE at saturation= 58.7%